

Product Features

- Compliant with QSFP-DD MSA Type2
- 4 CWDM lanes MUX/DEMUX design
Data rate 106.25Gbps per lane
- 100G Lambda MSA 400G FR4 Specification
Compliant
- Up to 2km transmission on single mode fiber
- Cooled EML Laser with PIN Receiver
- 8x53.125Gbps electrical interface(400GAUI-8)
- Single +3.3V power supply
- Maximum power consumption 12W
- Operating case temperature: 0°C to +70°C
- Duplex LC connector
- RoHS Compliant

Applications

- 400G Ethernet

Ordering Information

Table 1. Ordering Information

Part Number	Product Description
WM-A4QDC402F4C00	400G QSFP-DD FR4 2km CT

Description

WM-A4QDC402F4C00 is a high performance, low cost transceiver with duplex LC connector, which supports transmission distance up to 2km over SM fiber. On the transmitter side, the module converts 8 channels of 50Gbps (PAM4) electrical input data to 4 channels of CWDM optical signals, and multiplexes them into a single channel for 400Gbps optical transmission. On the receiver side, the module optically de-multiplexes a 400Gbps optical input into 4 channels of CWDM optical signals, and converts them to 8 channels of 50Gbps (PAM4) electrical output data. The module incorporates 4 independent channels on CWDM4 1271/1291/1311/1331nm center wavelength, operating at 100G per channel. The module supports commercial operating temperature, and the specification is compliant with 100G Lambda MSA 400G FR4 Technical Specification and the electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA.

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T _s	-40	85	°C
Relative Humidity	RH	5	85	%
Supply Voltage	V _{CC}	-0.5	3.6	V

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature(Commercial)	T _C	0	--	70	°C
Supply Voltage	V _{CC}	3.135	3.3	3.465	V
Data Rate Each Lane	--	--	26.5625	--	GBd
Link Distance	D	0.002		2	km

Transmitter Optical Characteristics

Table 4. Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
PAM4 Signaling rate, each lane	--	--	53.125 ± 100 ppm	--	GBd	--
Lane Wavelengths(range)	λ ₀	1264.5	1271	1277.5	nm	--
	λ ₁	1284.5	1291	1297.5		--
	λ ₂	1304.5	1311	1317.5		--
	λ ₃	1324.5	1331	1337.5		--
Side-mode suppression ratio	SMSR	30	--	--	dB	--
Total average launch power	--	--	--	9.3	dBm	--
Average launch power, each lane	Pa	-3.3	--	3.5	dBm	1
Outer Optical Modulation Amplitude, each lane	OMA _{outer}	-0.3	--	3.7	dBm	2
Difference in launch power between any two lanes (OMA _{outer})	--	--	--	4	dB	--
Launch power in OMA _{outer} minus TDECQ, each lane (min): for extinction ratio ≥ 4.5 dB for extinction ratio < 4.5 dB	--	-1.7 -1.6	--	--	dBm	--
Transmitter and dispersion penalty eye closure for PAM4 (TDECQ), each lane	TDECQ	--	--	3.4	dB	--

TDECQ – $10 \cdot \log_{10}(C_{eq})$, each lane	--	--	--	3.4	dB	4
Average launch power of OFF transmitter, each lane	P_{off}	--	--	-20	dBm	--
Extinction ratio	ER	3.5	--	--	dB	--
Transmitter transition time	--	--	--	17	ps	--
RIN17.1 OMA	RIN	--	--	-136	dB/Hz	--
Optical return loss tolerance	TOL	--	--	17.1	dB	--
Transmitter reflectance	T_{RL}	--	--	-26	dB	3
Notes: 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance. 2: Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMAouter (min) must exceed this value. 3: Transmitter reflectance is defined looking into the transmitter. 4: C_{eq} is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.						

Receiver Optical Characteristics

Table 5. Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
PAM4 Signaling rate, each lane	--	--	53.125 ± 100 ppm	--	GBd	--
Lane wavelengths	λ_0	1264.5	--	1277.5	nm	--
	λ_1	1284.5	--	1297.5	nm	--
	λ_2	1304.5	--	1317.5	nm	--
	λ_3	1324.5	--	1337.5	nm	--
Damage threshold, each lane	--	4.5	--	--	dBm	1
Average receive power, each lane	--	-7.3	--	3.5	dBm	2
Receive power, each lane (OMAouter)	--	--	--	3.7	dBm	--
Difference in receive power between any two lanes (OMAouter)	--	--	--	4.1	dB	--
Receiver reflectance	--	--	--	-26	dB	--
Receiver sensitivity (OMAouter), each lane	--	--	--	Equation (1)	dBm	3
Stressed receiver sensitivity (OMAouter), each lane	--	--	--	-2.6	dBm	4
Conditions of stressed receiver sensitivity test: Stressed eye closure for PAM4 (SECQ), lane under test SECQ – $10 \cdot \log_{10}(C_{eq})$, lane under test (max) OMAouter of each aggressor lane	--	--	3.4 1.5	3.4	dB dB dBm	5

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level. The receiver does not have to operate correctly at this input power.
2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver Sensitivity should meet Equation (1), which is illustrated in Figure1.

$$RS = \max(-4.6, \text{SECQ}-6.0) \text{ dBm} \quad (1)$$
4. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4}
5. Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.

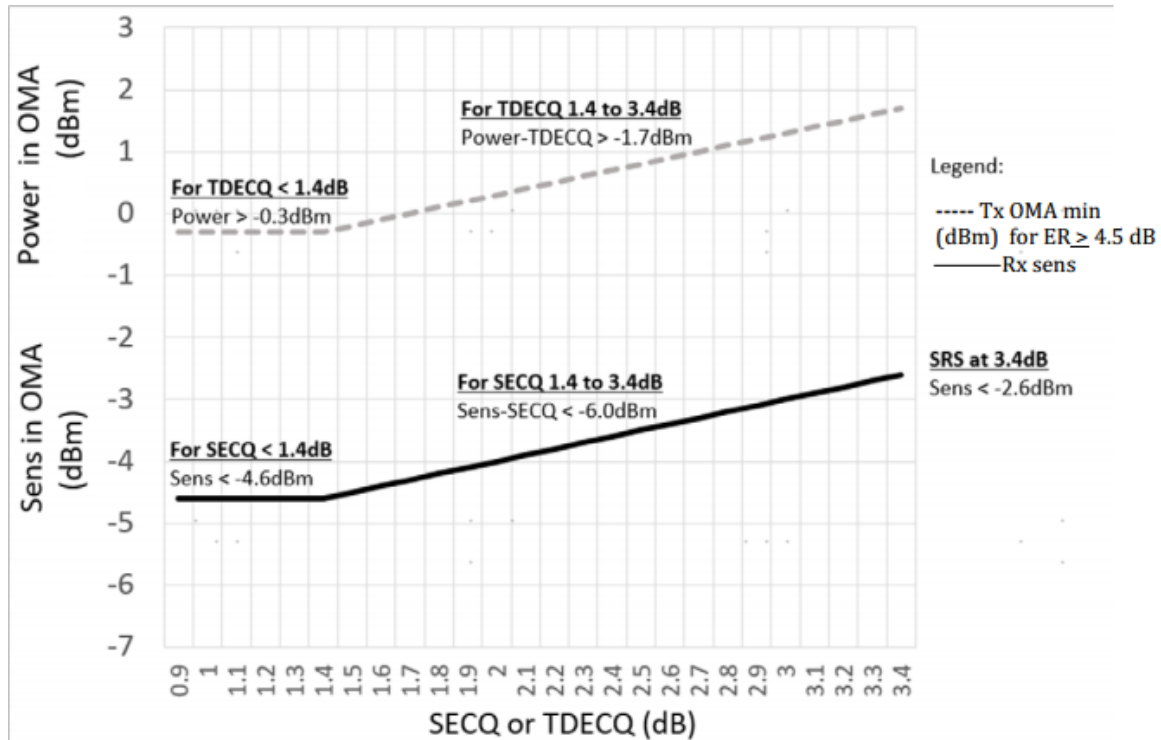


Figure1. Illustrated of receiver sensitivity mask for 400G FR4

Transceiver Electrical Characteristics

Table 6. Transceiver Electrical Characteristics

Parameter	Test Point	Minimum	Typical	Maximum	Unit	Notes
Module Supply Current	I _{cc}	--	--	3636	mA	--
Power Dissipation	P _D	--	--	12	W	--
Transmitter						
Signaling Rate, each Lane	--	26.5625±100ppm			GBd	--
Input Differential Impedance	Z _{IN}	--	100	--	Ω	--
Differential Data Input Swing	V _{IN} , P-P	210	--	900	mVP-P	1
Differential Termination Mismatch	TP1	--	--	10	%	--

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Parameter	Test Point	Minimum	Typical	Maximum	Unit	Notes
Differential Input Return Loss	TP1	IEEE 802.3 2015 Equation (83E-5)	--	--	dB	--
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)	--	--	dB	--
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1			--	2
Single-ended voltage tolerance range	TP1a	-0.4 to 3.3			V	--
DC common mode voltage	TP1	-350	--	2850	mV	3
Receiver						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	--
Output Differential Impedance	TP4	---	100	--	Ω	--
Differential termination mismatch	TP4	--	--	10	%	--
Differential Data Output Swing	TP4	--	--	900	mV _{P-P}	--
AC Common Mode Output Voltage, RMS	TP4	--	--	17.5	mV	--
Differential output return loss	TP4	IEEE 802.3-2015 Equation (83E-2)	--	--	--	--
Common to differential mode conversion	TP4	IEEE 802.3-2015 Equation (83E-3)	--	--	--	--
Near-end eye width, all 3 eyes	TP4	--	0.265	--	UI	--
Near-end eye height, all 3 eyes	TP4	--	70	--	mV	--
Far-end eye width, all 3 eyes	TP4	--	0.2	--	UI	--
Far-end eye height, all 3 eyes	TP4	--	30	--	mV	--
Far-end pre-cursor ISI ratio	TP4	-4.5	--	2.5	%	--
Transition time	TP4	9.5	--	--	ps	--
DC common mode voltage	TP1	-350	--	2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle
2. Meets BER specified in IEEE 802.3bs 120E.1.1
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage

Pin Description

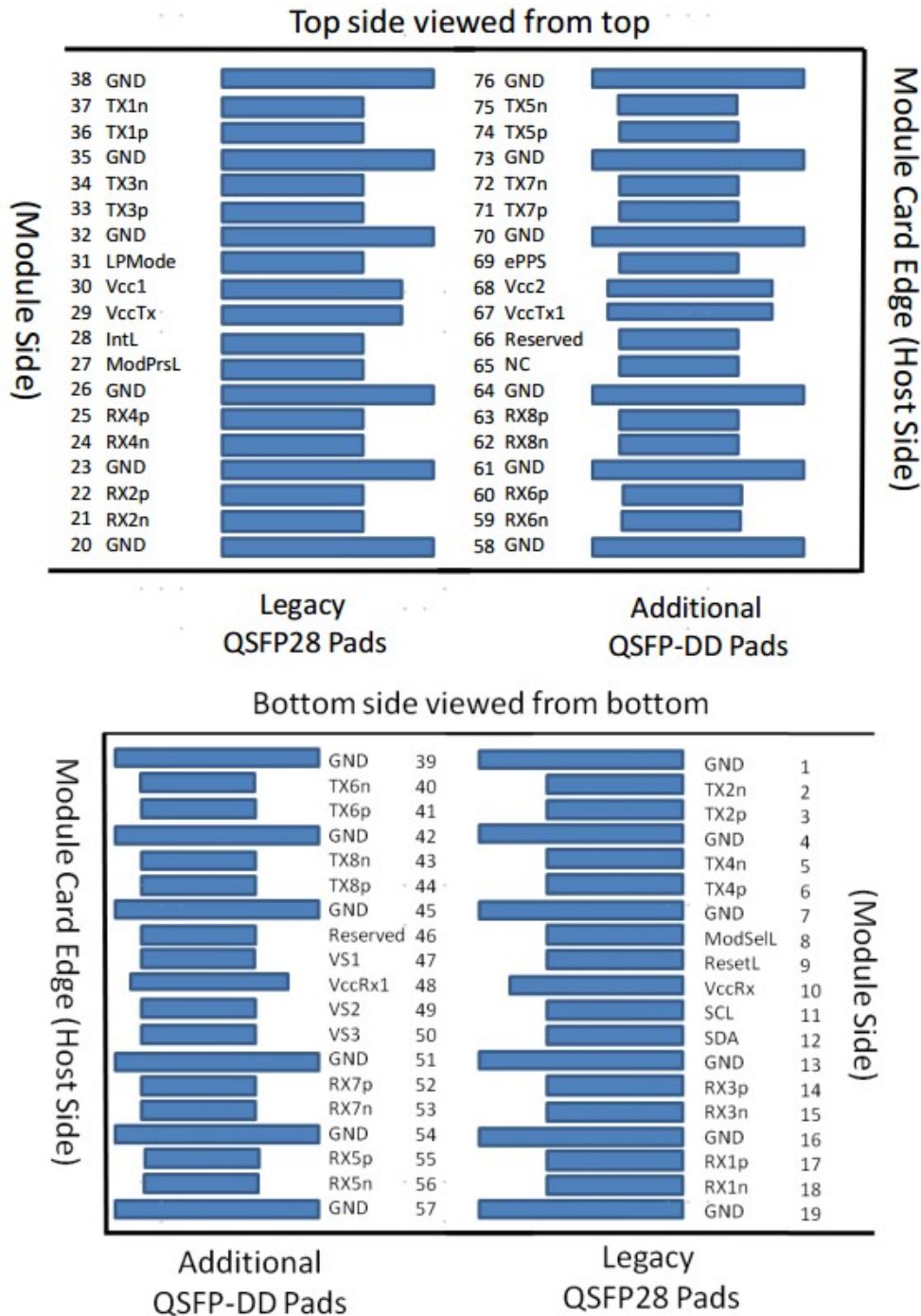


Figure 2. QSFP-DD pad assignment top view

Table 7. Pin Description

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1	--	GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	--
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	--
4	--	GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	--
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	--
7	--	GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	--
9	LVTTL-I	ResetL	Module Reset	3B	--
10	--	VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	--
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	--
13	--	GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	--
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	--
16	--	GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	--
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	--
19	--	GND	Ground	1B	1
20	--	GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	--
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	--
23	--	GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	--
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	--
26	--	GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	--
28	LVTTL-O	IntL	Interrupt	3B	--
29	--	VccTx	+3.3V Power supply transmitter	2B	2
30	--	Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	--
32	--	GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	--
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	--
35	--	GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	--
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	--
38	--	GND	Ground	1B	1
39	--	GND	Ground	1A	1

Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	--
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	--
42	--	GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	--
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	--
45	--	GND	Ground	1A	1
46	--	Reserved	For future use	3A	3
47	--	VS1	Module Vendor Specific 1	3A	3
48	--	VccRx1	3.3V Power Supply	2A	2
49	--	VS2	Module Vendor Specific 2	3A	3
50	--	VS3	Module Vendor Specific 3	3A	3
51	--	GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	--
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	--
54	--	GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	--
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	--
57	--	GND	Ground	1A	1
58	--	GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	--
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	--
61	--	GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	--
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	--
64	--	GND	Ground	1A	1
65	--	NC	No Connect	3A	3
66	--	Reserved	For future use	3A	3
67	--	VccTx1	3.3V Power Supply	2A	2
68	--	Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70	--	GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	--
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	--
73	--	GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	--
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	--
76	--	GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 8. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may

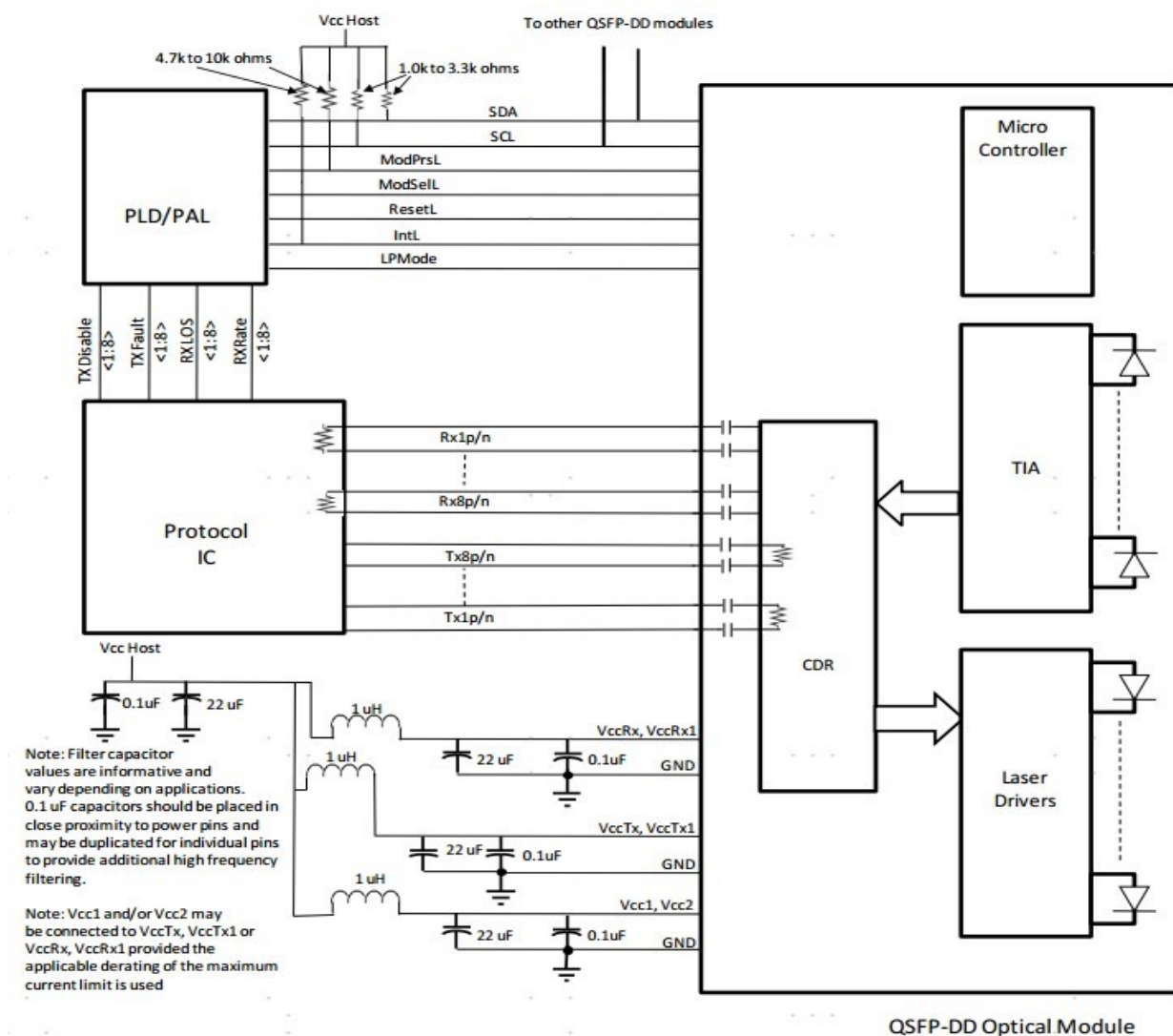
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be internally connected within the module in any combination. For power classes 4 and above the module differential loading of input voltage pins must not result in exceeding pin current limits. The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 ohm to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k Ω and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B

Recommended peripheral circuit



Outline Dimensions

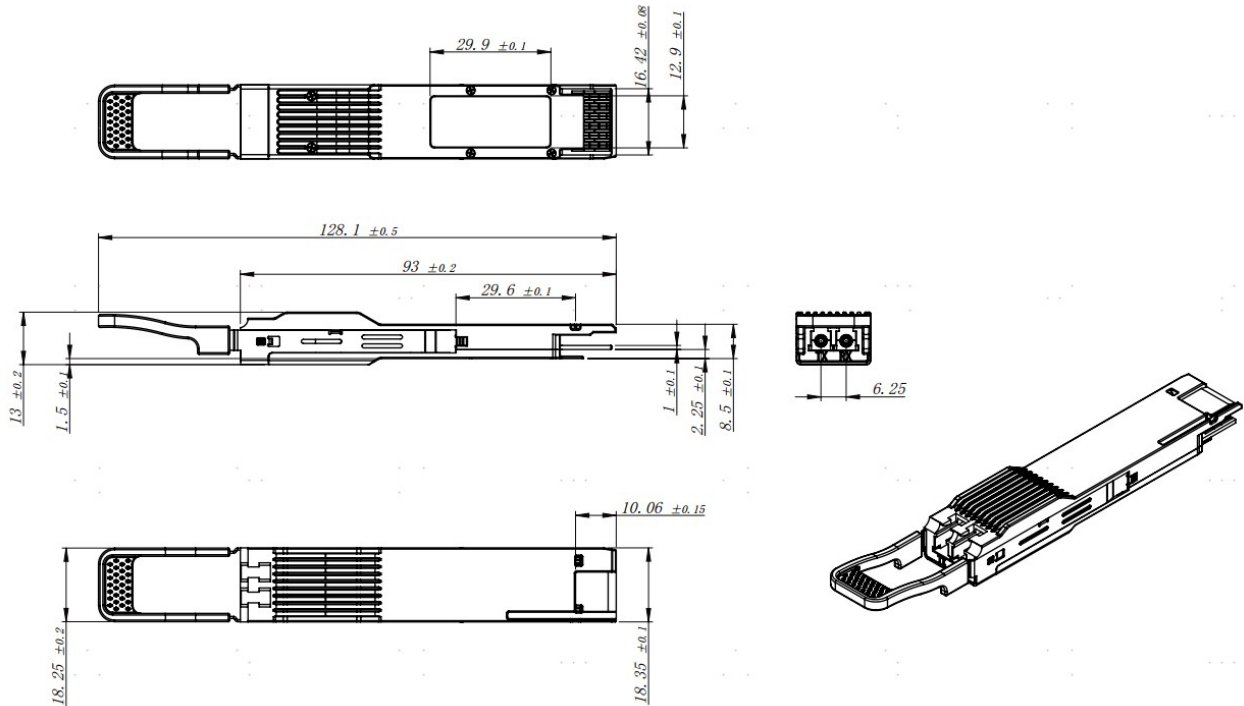


Figure 4. Outline Dimensions

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